<u>**In The Specification:**</u>

The paragraph [0035] in the specification is corrected as follows:

-- As depicted in the block diagrams shown in Fig. 3 and Fig. 4, three display devices co-operating by the same clock source are connected to a computer system that contains a system memory directly accessed by the CPU. The three display devices may run in different refresh frequencies, thereby three different frequencies of display-device blank periods, and after the display devices has been stabilized, a least common multiple occurrence of the device blank periods can be found periodically as depicted in the timing diagram shown in Fig. 5. Fig. 6 that demonstrates the mechanism of the first preferred embodiment by a flow chart diagram. The mechanism first applies the same operation clock source to the display devices in step 601 and program the three display devices to have simple fraction timing relationship to synchronize their vertical signals, horizontal signals, and blank periods in step 602. Then, the mechanism waits to receive a power saving process signal that sends from the CPU and indicates a request for executing the power saving process by the CPU, and acquires the length of a power saving process period (PSPP) in step 603. During the PSPP, the CPU of the computer system idles to wait for a change of operating clock frequency, thereby the CPU falling into a non-responding period, and blocking the memory access from a graphics-processing unit to a system memory. Once the power saving process signal has <u>been</u> received and the length of the PSPP has <u>been</u> obtained, the mechanism detects the upcoming least common multiple occurrence of the display-device blank periods in step 604; and executes the power saving process within the least common multiple occurrence of the display-device blank periods in step 605. After the power saving

process has finished, the mechanism goes back to the state of waiting to receive the next power

saving process signal in step 603. --